## REMARKS

Claims 1, 3 - 13, 15 - 21, 32, 33 and 35 - 47 are pending in the present application. Claims 22 - 31 were previously canceled. Claims 2, 14 and 34 are canceled by the present amendment. Reconsideration of the application is respectfully requested.

Applicant is amending the specification to correct some typographical errors.

In section 3 of the Office Action, claims 2, 14, and 34 are rejected. Claims 2, 14 and 34 are canceled, as mentioned above. Withdrawal of the rejection is respectfully solicited.

In section 5 of the Office Action, claims 1, 3, 5 - 8, 11 - 13, 15, 18 - 21, 32, 33, 35, 38 - 42, 46 and 47 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Application Publication No. 2001/0040631 to Ewedemi et al. (hereinafter "the Ewedemi et al. publication"). Applicant is clarifying an aspect of claims 1, 11 and 32 that is not disclosed by the Ewedemi et al. publication.

Claim 1 provides for a circuit that includes, *inter alia*, a decoder for converting a memory address into a row signal to drive a row of an active pixel sensor array, and a column signal to drive a column of the active pixel sensor array.

FIG. 1 of the present application is a block diagram of a random access imaging sensor 100 that includes an array decoder logic 6, a row decoder 4, a column decoder 5, and a digital control interface 7. Digital control interface 7 receives an address from a microprocessor 3 and passes the address to array decoder logic 6. Array decoder logic 6 converts the address into a row signal and a column signal, and via row decoder 4 and column decoder 5, drives a row and a column of pixel matrix 2.

The Ewedemi et al. publication, with reference to FIG. 2, discloses an image sensor 100 that includes a sensor array 102, a local memory 110, and an interface protocol conversion circuit 114. Sensor readout from sensor array 102 is stored in local memory 110, and interface protocol conversion

circuit 114 provides a memory interface for exporting pixel data stored in local memory 110 (par. 0032). More specifically, interface protocol conversion circuit 114 provides a translation of memory interface protocols between local memory 110 and an image processing unit 20 (par. 0033).

Note that FIG. 2 of the Ewedemi et al. publication shows a directed line from interface protocol conversion circuit 114 to local memory 110, but does not show any line from interface protocol conversion circuit 114 to sensor array 102. Interface protocol conversion circuit 114 apparently converts a memory address from image processing unit 20 into an address of data in local memory 110. Interface protocol conversion circuit 114 does not convert a memory address from image processing unit 20 into a row signal to drive a row of sensor array 102, and a column signal to drive a column of sensor array 102.

The Ewedemi et al. publication, with reference to FIG. 3, discloses an image sensor 200 that includes a pixel array 202, a local memory 210, and an interface protocol conversion circuit 214, and indicates that the operation of image sensor 200 is similar to that of image sensor 100 if FIG. 2 (par. 0034). Thus, interface protocol conversion circuit 214 apparently converts a memory address from image processing unit 20 into an address of data in local memory 210. FIG. 3 does not show any line from interface protocol conversion circuit 214 to pixel array 202. Interface protocol conversion circuit 214 does not convert a memory address from image processing unit 20 into a row signal to drive a row of pixel array 202, and a column signal to drive a column of pixel array 202.

The Office Action suggests that the Ewedemi et al. publication's interface protocol conversion circuit 214 is a disclosure of the decoder of claim 1. However, whereas interface protocol conversion circuit 214 apparently converts a memory address from image processing unit 20 into an address of data in local memory 210, interface protocol conversion circuit 214 does not convert a memory address from image processing unit 20 into a row signal to drive a row of pixel array 202, and a column signal to drive a column of pixel array 202. Therefore, the Ewedemi et al. publication does not disclose a decoder for converting a memory address into **a row signal to drive a row of an active pixel sensor**

**array, and a column signal to drive a column of the active pixel sensor array**, as recited in claim 1. Thus, the Ewedemi et al. publication does not anticipate claim 1.

Claims 3 and 5 - 8 depend from claim 1. By virtue of this dependence, claims 3 and 5 - 8 are also novel over the Ewedemi et al. publication.

Claim 11 is an independent claim, and includes a recital similar to that of claim 1, as described above. Accordingly, claim 11, for reasoning similar to that provided in support of claim 1, is novel over the Ewedemi et al. publication.

Claims 12, 13, 15 and 18 - 21 depend from claim 11. By virtue of this dependence, claims 12, 13, 15 and 18 - 21 are also novel over the Ewedemi et al. publication.

Claim 32 is an independent claim, and includes a recital similar to that of claim 1, as described above. Accordingly, claim 32, for reasoning similar to that provided in support of claim 1, is novel over the Ewedemi et al. publication.

Claims 33, 35, and 38 - 42 depend from claim 32. By virtue of this dependence, claims 33, 35, and 38 - 42 are also novel over the Ewedemi et al. publication.

Claims 46 and 47 depend from claim 1. By virtue of this dependence, claims 46 and 47 are also novel over the Ewedemi et al. publication.

Applicant respectfully requests reconsideration and withdrawal of the rejection set forth in section 5 of the Office Action.

In section 7 of the Office Action, claims 1, 3, 5 - 8, 11 - 13, 15, 18 - 21, 32, 33, 35, 38 - 42, 46 and 47 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,512,218 to Canini et al. (hereinafter "the Canini et al. patent"). Applicant is traversing this rejection.

In claim 1, the decoder, in addition to the features mentioned above, is also for receiving a memory address within a memory address space of a processor.

The Canini et al. patent discloses a circuit that includes a logic control unit 10. The Office Action suggests that logic control unit 10 is a disclosure of the decoder of claim 1. Applicant respectfully disagrees.

In the Canini et al. patent, a microprocessor 15[1] is connected to logic control unit 10 via a line 18 that supplies control signals to logic control unit 10 (col. 3, lines 59 - 61). The Canini et al. patent does not describe the control signals as being a memory address. However, the Canini et al. patent does mention address operations, but in this regard **expressly distinguishes between addresses and control signals** (col. 5, line 59), and **expressly identifies an address bus** (col. 5, line 26). Therefore, line 18 does not supply a memory address to logic control unit 10, and so, logic control unit 10 does not receive a memory address within a memory address space of microprocessor 15. Consequently, the Canini et al. patent does not disclose a decoder for receiving **a memory address within a memory address space of a processor**, as recited in claim 1. Accordingly, the Canini et al. patent does not anticipate claim 1.

On page 4 of the Office Action, the Examiner states that the features of claim 1 "are inherent since Canini et al. carries out direct memory access, which Applicant equates to a processor addressing a pixel array within the memory space of the processor." Applicant respectfully disagrees with the Examiner's position, and below, explains that the features of claim 1 are not inherent to the system of the Canini et al. patent.

The Canini et al. patent, with reference to FIG. 6, discloses a system that includes a direct memory access (DMA) controller 30 (col. 5, lines 43 - 45). In the implementation shown in FIG. 6,

[1] The Canini et al. patent, at col. 3, lines 59 - 60, erroneously identifies the microprocessor with reference number 13 rather than reference number 15.

pixel data from CMOS sensor 5 is moved from A/D converter 7, by DMA controller 30 to a RAM memory 17. In a system that employs the circuit of claim 1 of the present application, since the decoder receives a memory address within the memory address space of a microprocessor, the microprocessor can access pixel data from an image sensor as if the image sensor was in the memory space of the microprocessor. Therefore, when using the circuit of claim 1, the pixel data can be moved to the microprocessor's accumulator by accessing an area of memory within the microprocessor's memory space. In order for this to happen in the system of the Canini et al. patent, an address bus that connects ROM 16 or RAM 17 to microprocessor 15 would need to be connected directly to logic control unit 10. The Canini et al. patent does not show such a connection, and it does not describe or suggest any operation of accessing CMOS sensor 5 as if CMOS sensor 5 was in the memory space of microprocessor 15. Moreover, as explained above, in the Canini et al. patent, logic control unit 10 receives control signals from microprocessor 15. Therefore, in the Canini et al. patent, there is no inherent reason for logic control unit 10 to receive a memory address within the memory address space of microprocessor 15. Thus, the Canini et al. patent neither discloses nor suggests a decoder for **receiving a memory address within a memory address space of a processor**, as recited in claim 1.

Claims 3 and 5 - 8 depend from claim 1. By virtue of this dependence, claims 3 and 5 - 8 are also novel over the Canini et al. patent.

Claim 11 is an independent claim, and includes a recital similar to that of claim 1, as described above. Accordingly, claim 11, for reasoning similar to that provided in support of claim 1, is novel over the Canini et al. patent.

Claims 12, 13, 15 and 18 - 21 depend from claim 11. By virtue of this dependence, claims 12, 13, 15 and 18 - 21 are also novel over the Canini et al. patent.

Claim 32 is an independent claim, and includes a recital similar to that of claim 1, as described above. Accordingly, claim 32, for reasoning similar to that provided in support of claim 1, is novel over the Canini et al. patent.

Claims 33, 35, and 38 - 42 depend from claim 32. By virtue of this dependence, claims 33, 35, and 38 - 42 are also novel over the Canini et al. patent.

Claims 46 and 47 depend from claim 1. By virtue of this dependence, claims 46 and 47 are also novel over the Canini et al. patent.

Applicant respectfully requests reconsideration and withdrawal of the rejection set forth in section 7 of the Office Action.

In section 9 of the Office Action, claims 4, 16, 17, 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over either one of the Ewedemi et al. publication or the Canini et al. patent, in view of U.S. Patent No. 5,626,871 to Wilder et al. (hereinafter "the Wilder et al. patent"). Applicant is traversing this rejection.

Claim 4 depends from claim 1. Claims 16 and 17 depend from claim 11. Claims 36 and 37 depend from claim 32. Above, Applicant explained that claims 1, 11 and 32 are novel over both of the Ewedemi et al. publication and the Canini et al. patent. Applicant submits that the Wilder et al. patent does not make up for the deficiencies of the Ewedemi et al. publication and the Canini et al. patent, as they relate to claims 1, 11, and 32. Accordingly, Applicant submits that claims 1, 11 and 32, and claims 4, 16, 17, 36 and 37, by virtue of their dependencies, are all patentable over the cited combinations of the Ewedemi et al. publication, the Canini et al. patent, and the Wilder et al patent.

Applicant respectfully requests reconsideration and withdrawal of the rejection set forth in section 9 of the Office Action.

In section 10 of the Office Action, claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over either one of the Ewedemi et al. publication or the Canini et al. patent. Applicant is traversing this rejection.

Claims 9 and 10 depend from claim 1. Above, Applicant explained that claim 1 is novel over both of the Ewedemi et al. publication and the Canini et al. patent. Applicants further submit that neither of the Ewedemi et al. publication nor the Canini et al. patent suggests all of the features of claim 1. Accordingly, Applicant further submits that claim 1, and claims 9 and 10 by virtue of their dependence on claim 1, are all patentable over the Ewedemi et al. publication and the Canini et al. patent.

Applicant respectfully requests reconsideration and withdrawal of the rejection set forth in section 10 of the Office Action.

In section 11 of the Office Action, claims 43 - 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over either one of the Ewedemi et al. publication or the Canini et al. patent, in view of U.S. Patent No. 6,825,936 to Metcalfe et al. (hereinafter "the Metcalfe et al. patent"). Applicant is traversing this rejection.

Claims 43 - 45 depend from claim 32. Above, Applicant explained that claim 32 is novel over both of the Ewedemi et al. publication and the Canini et al. patent. Applicant respectfully submits that the Metcalfe et al. patent does not make up for the deficiency of the Ewedemi et al. publication and the Canini et al. patent, as they relate to claim 32. Accordingly, Applicant further submits that claim 32, and claims 43 - 45 by virtue of their dependency on claim 32, are all patentable over the cited combinations of the Ewedemi et al. publication, the Canini et al. patent, and the Metcalfe et al. patent.

Applicant respectfully requests reconsideration and withdrawal of the rejection set forth in section 11 of the Office Action.

As mentioned above, Applicant is clarifying an aspect of claims 1, 11 and 32 that is not disclosed by the Ewedemi et al. publication. Applicant amended claim 47 for consistency with claim 1. None of

the amendments is intended to narrow the meaning of any term of any of the claims, and therefore, the doctrine of equivalents should be available for all of the terms of all of the claims.

In view of the foregoing, Applicant respectfully submits that all claims presented in this application patentably distinguish over the prior art. Accordingly, Applicant respectfully requests favorable consideration and that this application be passed to allowance.

Respectfully submitted,

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Date

Paul D. Greeley
Reg. No. 31,019
Attorney for the Applicant
Ohlandt, Greeley, Ruggiero & Perle, L.L.P.
One Landmark Square, 10th Floor
Stamford, CT 06901-2682
Tel: 203-327-4500
Fax: 203-327-6401